A 24GHz Down-Conversion Mixer with Low Noise and High Gain

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Abstract—In this paper, a down-converting mixer implemented in the TSMC 0.18-μm CMOS process technology for applications in the 24GHz band is presented. For suppressing the flicker noise generated in the switching stage of the conventional Gilbert cell topology, a current bleeding technique combined with negative resistance is adopted to improve the noise figure (NF) of the mixer. In addition, an inductor is utilized to resonate with the parasitic capacitances at the output of the transconductance (Gm) stage and thus increases the power conversion gain (CG) and the linearity of the proposed mixer. The chip size of the proposed mixer is 1.062 × 0.979 mm², and the core circuit consumes a dc power of 5.65mW from the 1.8-V voltage supply. The measured CG and NF for the proposed 24GHz mixer are 8.376dB and 11.6dB, respectively. And the measured 1dB compression point (P1dB) is –8.4dBm at the 24GHz operating frequency.

Keywords—CMOS; current bleeding technique; Gilbert cell; K band

I. INTRODUCTION

The growing demand of data transfer via the wireless communication systems results in the fast development of various portable products. Some systems operating above 20 GHz, including the vehicle crash prevention radars, wireless local area networks, local multipoint distribution service (LMDS), and other ISM band applications, have been proposed. In those systems, the RF front-end circuits are crucial and the design trend is with low chip cost and low power consumption. One of the critical RF front-end circuits is the mixer which converts the incoming RF signal to the intermediate frequency (IF) signal. The mixer in general is the second or third stage, and it is required to provide a sufficient power conversion gain (CG) with low noise figure (NF) and high linearity.

A double balanced mixer (Gilbert cell) as shown in Fig. 1 is commonly used in receivers, which has less even-order distortion and low LO-IF feedthrough. The noise figure of a mixer is influenced by many factors, including the noises from the Gm stage, the switching stage, and the load. The detailed analysis of the noise effect in a mixer design can be found in some previous contributions [1], [2]. Among those noise sources, a noise cancellation technique has been proposed to improve noise from the switching stage [3].

A direct conversion receiver, the flicker noise deeply affects the mixer’s noise performance in the close-in frequencies, and it is reported using current bleeding circuit with resonating inductor to overcome drawbacks introduced in switching stage [4], [5]. In this paper, we adopt the PMOS current bleeding technique with one resonating inductor and design a 24GHz mixer in the 0.18μm CMOS process technology.

Figure 1. Schematic of a conventional double-balanced mixer.

II. CIRCUIT DESIGN

The conventional double-balanced mixer (Gilbert cell) is as shown in Fig. 1. It consists of the transconductance (Gm) stage (formed by M1 and M2), the switching stage (formed by M3~M6), and load resistors (R1 and R2). In the mixer design, the specifications to be achieved are high gain, high linearity, low noise figure and low power consumption. However, these performances are difficult to achieve simultaneously. For example, we may achieve a higher gain at the cost of larger power consumption. Another example is that larger current in Gm stage can provide higher gain and suppress the noise, but also generate larger noise in switching stage. In addition, larger current will also diminish the voltage headroom due to the cascaded structure, thus the linearity is getting worse.

Noise is presented in all components including transistors and resistors. For a direct conversion receiver, the RF signal is down-converted directly to the DC. Because the flicker noise...
has a spectrum density distribution proportional to $1/f$, its contribution to overall system becomes significant at close-in frequencies. As indicated in [1], the flicker noises of mixers are primarily determined by LO switching pair devices, because the noise directly leaks to the output in process of frequency translation. Following the derivation in [1], the average value of the flicker noise current in outputs generated by switching pair devices in one period is

$$T_{\text{on}} = \frac{2}{T} \times 2I \times \frac{V_n}{S} = 4I \times \frac{V_n}{S \times T},$$

where $T$ is the period of the LO signal, $I$ is the dc bias current from the Gm stage, $V_n$ is the average flicker noise voltage of the switching pair, and $S$ is the slope of the LO signal. As explanation in [1], the flicker noise current in (1) appears at the output directly as low frequency noise and it modulates the zero-crossing point of the LO signal. From (1), the flicker noise can be reduced by either decreasing the dc current $I$ or increasing the slope of the LO signal.

The current bleeding technique can be implemented by using PMOS current source because the PMOS brings lower flicker noise. However, the current bleeding technique suffers some drawbacks which limit its improvement on the mixer. First, there exist parasitic capacitances at the node between Gm stage and switching stage, which will shunt the RF current from the Gm stage to the ground node. The current bleeding circuit will produce additional parasitic capacitances at that node, and it leads to more loss of the RF signal. Therefore, the conversion gain will drop down and the noise figure will increase. Secondly, the current bleeding circuit consists of active devices which also produce noises and make the noise figure of the mixer worse. For these reasons, the improvement by using the primitive current bleeding technique is not significant. Since additional parasitic capacitances introduced by the current bleeding circuit are the main factor diminishing its benefit, thus it was proposed to resonate out the parasitic capacitances by adding one inductor between the current injection nodes [4], [5]. The advantages of this modification include not only improving flicker noises but also enhancing the conversion gain.

Although we can use PMOS devices which generate less flicker noises compared to NMOS, the current bleeding circuit contributes additional noises. It is reported that the current bleeding circuit may use PMOS transistors to form cross-coupled pair which can cancel the noises [3]. Such technique can also generate negative resistance at the output of the Gm stage which boosts the small signal voltage gain. We combine the cross-coupled pair technique with the inductor mentioned above and design a mixer for 24GHz applications as shown in Fig. 3. The inductor $L_5$ is used for resonating out the parasitic capacitances and PMOS $M_7$ and $M_8$ form the cross-coupled pair for providing the bleeding current. Inductors $L_1$, $L_2$, $L_3$, and $L_4$ are used for input matching to 50 Ohms, and this matching method also take the noise figure into account. Since inductors $L_3$ and $L_4$ are also used as inductive source-degeneration, it can thus help the linearity performance. Fig. 4 shows the chip micrograph of the proposed mixer which is implemented in 0.18μm CMOS process technology and the chip size is 1.062×0.979 mm².
III. MEASURED RESULTS

The core circuit of the proposed mixer draws a 5.65mW dc power from a 1.8V power supply. Fig. 5 shows the measured power gain and output power with respect to LO input power of the mixer at 24GHz operating frequency. It can be seen that the gain will reach the saturated level $8.2$dB at the LO input level of $-2$dBm. Thus we choose the LO signal power level as $-2$dBm for other measurements. Fig. 6 shows the measured P1dB and it reads $-8.4$dBm. Fig. 7 shows the measured NF and CG versus the IF frequency, in which the NF and CG are 11.6 dB and 8.376dB, respectively, for the IF frequency being 50MHz. A summary of the performance of the proposed mixer is listed in Table I and some results of previous works for 24GHz applications [7]-[9] are also given in this table. For a fair comparison, we adopt the figure of merit (FOM) formula similar to that given in [10] with IIP3 replaced by P1dB as shown below the Table I. It can be seen that the performances of our mixer are superior to those in [7]-[9].

IV. CONCLUSIONS

We have presented a direct down conversion Gilbert mixer with the dynamic current bleeding technique and an inductor for resonating parasitic capacitances. The circuit is designed in the 0.18μm CMOS process technology. The core circuit draws 5.65mW dc power consumption from the 1.8-V power supply. The measured conversion gain and NF are 8.376dB and 11.6dB, respectively, for the IF frequency being 50MHz. The measured P1dB is $-8.4$dBm for the RF frequency being 24GHz. The performance of the proposed mixer shows its superiority by comparing with previous works for 24GHz applications.

ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center (CIC) in Hsinchu, Taiwan for the chip fabrication, measurement and other technical supports.
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\[
\text{FOM} = 10 \log \left( \frac{10^{0.25} \cdot 10^{0.10}}{10^{0.35} \cdot P} \right)
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in which, \( P \) = DC power consumption in W.

REFERENCES


